Abstract of the Disclosure

A method of arbitrating a system bus shared by a CPU, which is a first master device,, and second and third master devices comprises storing a first bus occupancy rate for each master device and a variable bus occupancy rate.   When an interrupt signal provided to the CPU is activated, a second rate for the CPU, which is a sum of the first rate for the CPU and the variable rate, and the first rates for the second and third master devices are applied to a bus arbiter.   When the interrupt signal is inactivated, a third rate for the CPU, which is obtained by subtracting the variable rate from the first rate for the CPU, and the first rates for the second and third master devices are applied to the bus arbiter.   A use priority of the system bus is controlled according to the rates applied to the bus arbiter.